ductor substrate, and a respective plurality of gate impurity regions of a second conductivity type in the epitaxial layer,

the gate impurity regions of the plurality of structures being formed in correspondence with each other so as to be coupled from each structure to the next;

after forming each structure, subjecting the structure to activation annealing, with each structure other than an uppermost structure of the plurality of structures being subjected to the activation annealing prior to forming the next structure; and

forming a source region between adjacent gate impurity regions of the uppermost structure,

wherein the gate impurity regions of the uppermost structure are arranged with a greater spacing than a spacing between the gate impurity regions of a preceding structure.

7. A method of manufacturing a junction field effect transistor according to claim **6**, wherein the activation annealing of at least some of the plurality of structures is performed in a state where the first main surface of the semiconductor substrate is covered with a carbon-based film.

8. A method of manufacturing a junction field effect transistor according to claim **6**, wherein the activation annealing of all of the plurality of structures is performed in a state where the first main surface of the semiconductor substrate is covered with a carbon-based film.

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